ABSTRACT OF THE DISCLOSURE

[0030] In some embodiments, systems and methods for sequencing multiple write state machines may comprise a pulse generator, a delay circuit, and a stacked memory array, wherein each memory array in the stacked memory array may have an individual write state machine. In an exemplary embodiment, the pulse generator may be operable to supply pulses of current to the write state machines so that the system's voltage regulator may accommodate the total aggregated current in the system. In some exemplary embodiments, pulses of current may be applied to the first write machine, and delayed pulses of current may be applied to the second write state machine. Other embodiments are described and claimed